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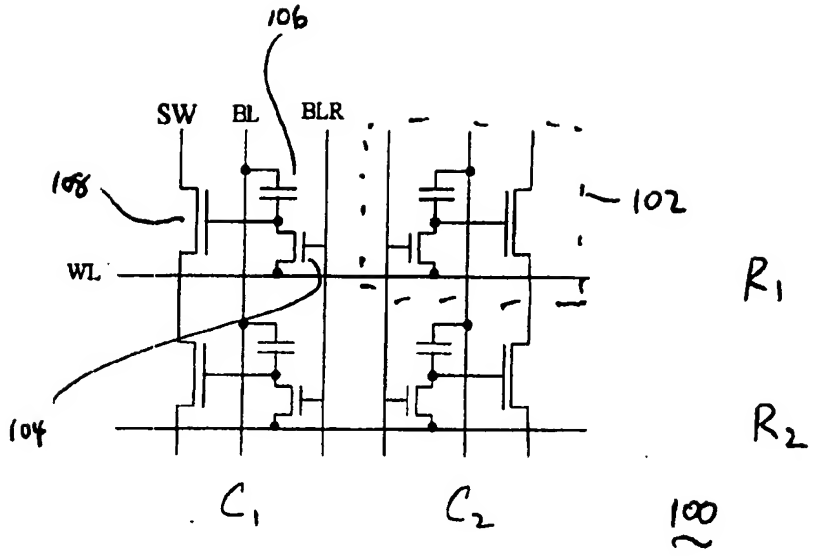

Fig. 1

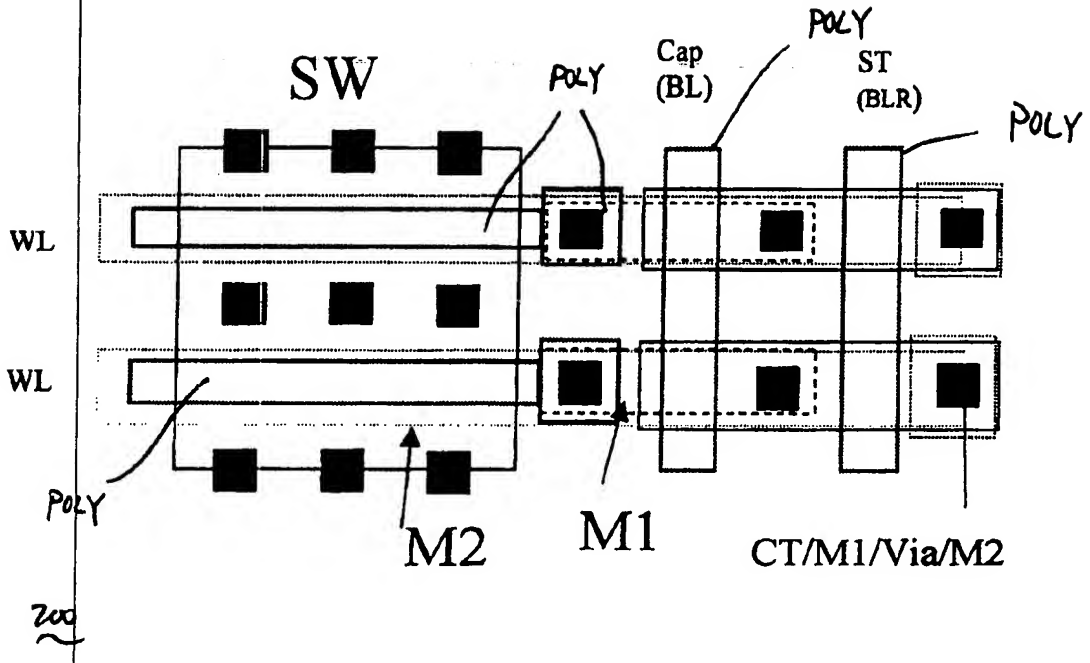

Fig 2

0.18um LV XPM FPGA Cell Operation

		Vbl	Vblr	Vwl			Program	
Program	SC/SR	8	3.3	0			Yes	301
	SC/UR	8	3.3	3.3			No	303
	UC/SR	0	0	0			No	305
	UC/UR	0	0	3.3			No	307
Read	SC/SR	1.8-3.3	1.8	0			Sense current	
	SC/UR	1.8-3.3	1.8	1.8			Yes	309
	UC/SR	0	0	0			No	311
	UC/UR	0	0	1.8			No	313
							No	315
Operation		1.8	0~0.8	0				
								317

Fig 3

0.18um IO XPM FPGA Cell Operation

		Vbl	Vbr	Vwl			Program	
Program	SC/SR	8	3.3	0			Yes	401
	SC/UR	8	3.3	3.3			No	403
	UC/SR	0	0	0			No	405
	UC/UR	0	0	3.3			No	407
Read	SC/SR	3.3	3.3	0			Sense current	
	SC/UR	3.3	3.3	3.3			Yes	409
	UC/SR	0	0	0			No	411
	UC/UR	0	0	3.3			No	413
							No	415
Operation		3.3	0.3~0.8	0				
							Yes	417

Fig 4

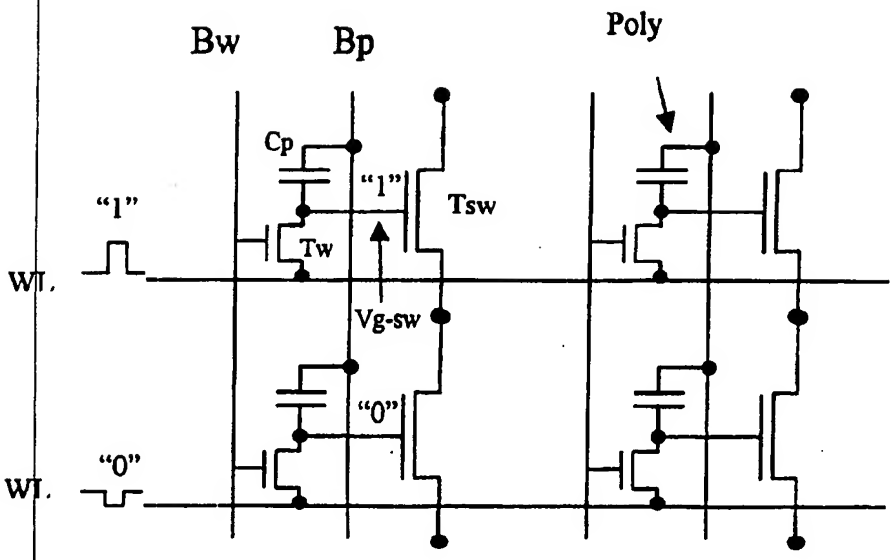

Fig 5

Dynamic XPM FPGA Cell Operation

		Vbw	Vbp	Vwl(1)	Vwl(0)
Write or Refreshing by columns	SC	Vcc	0	Vcc	0
	UC	0	0	Vcc	0

*SC- Selected Column; UC- unselected Column.

Fig 6

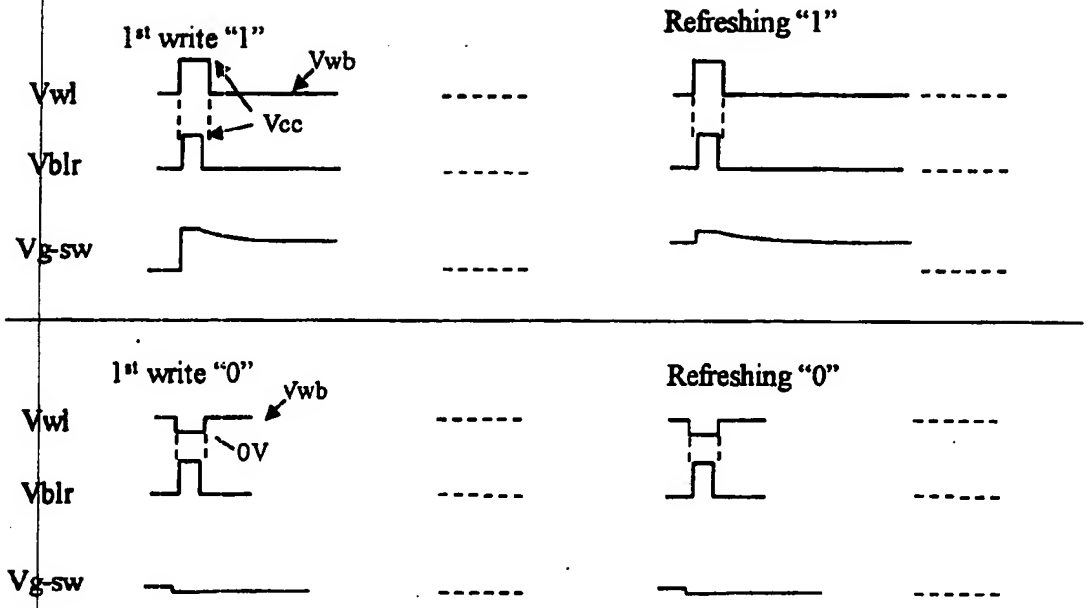
1st write "1"
Refreshing "1"
Vwb
Vcc
Vwl
Vblr
Vg-sw
1st write "0"
Refreshing "0"
Vwb
0V
Vwl
Vblr
Vg-sw

Fig 7

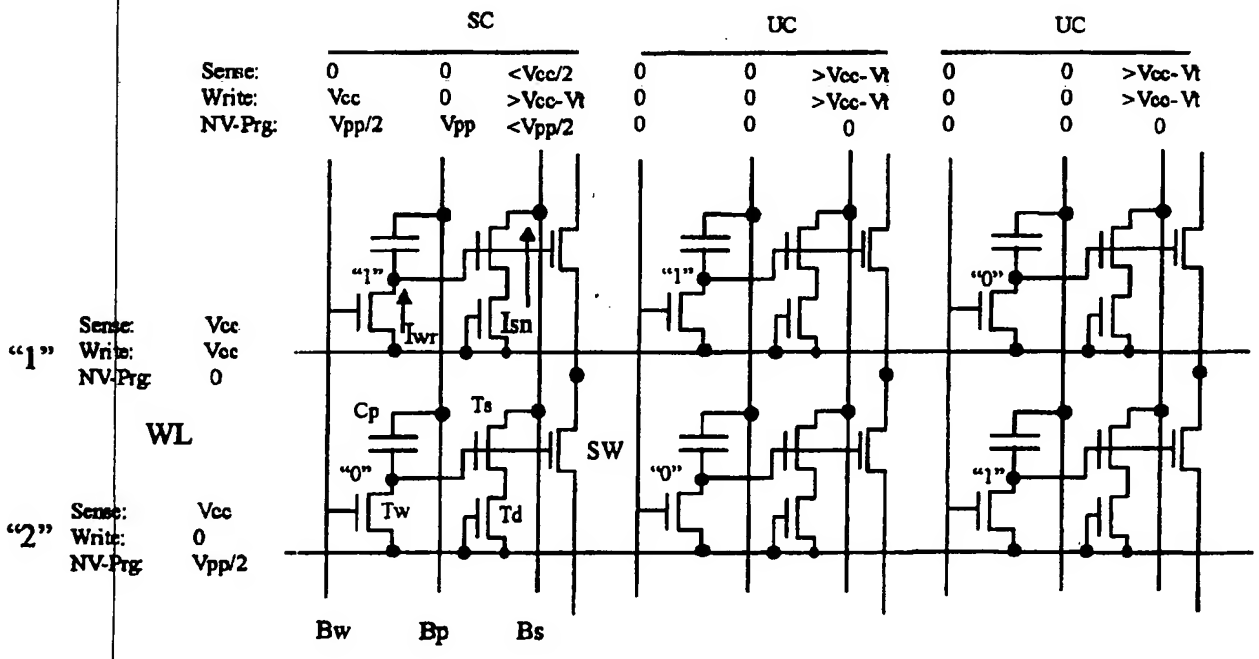
SC
UC
UC
Sense: 0 0 <Vcc/2 0 0 >Vcc-Vt 0 0 >Vcc-Vt
Write: Vcc 0 >Vcc-Vt 0 0 >Vcc-Vt 0 0 >Vcc-Vt
NV-Prg: Vpp/2 Vpp <Vpp/2 0 0 0 0 0 0
"1"
Sense: Vcc
Write: Vcc
NV-Prg 0
WL
"2"
Sense: Vcc
Write: 0
NV-Prg Vpp/2
"1"
Twr
Isn
Cp
Ts
"0"
Tw
Td
SW
"0"
"1"
"0"
"1"
"0"
Bw
Bp
Bs

Fig 8

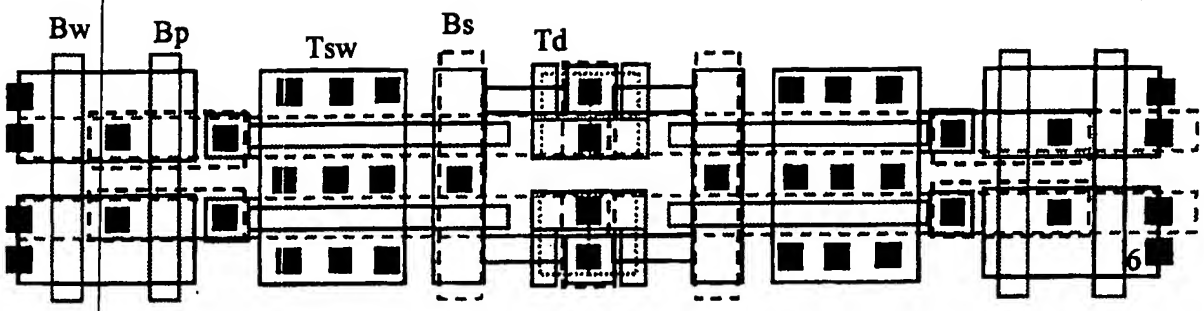
Bw
Bp
Tsw
Bs
Td
6

Fig 9

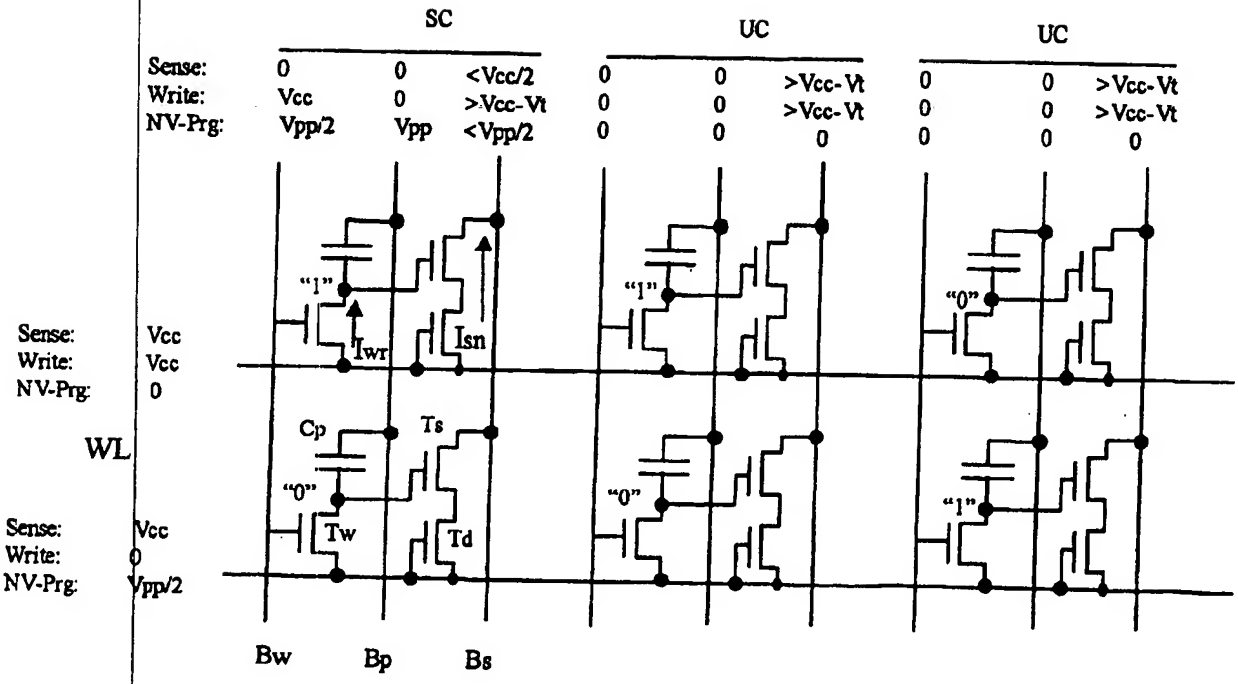
SC
UC
UC
Sense: 0 0 <Vcc/2 0 0 >Vcc-Vt 0 0 >Vcc-Vt
Write: Vcc 0 >Vcc-Vt 0 0 >Vcc-Vt 0 0 >Vcc-Vt
NV-Prg: Vpp/2 Vpp <Vpp/2 0 0 0 0 0 0
"1"
Twr
Isn
"1"
"0"
Sense: Vcc
Write: Vcc
NV-Prg: 0
WL
Cp
Ts
"0"
Tw
Td
"0"
"1"
Sense: Vcc
Write: 0
NV-Prg: Vpp/2
Bw
Bp
Bs

Fig 10

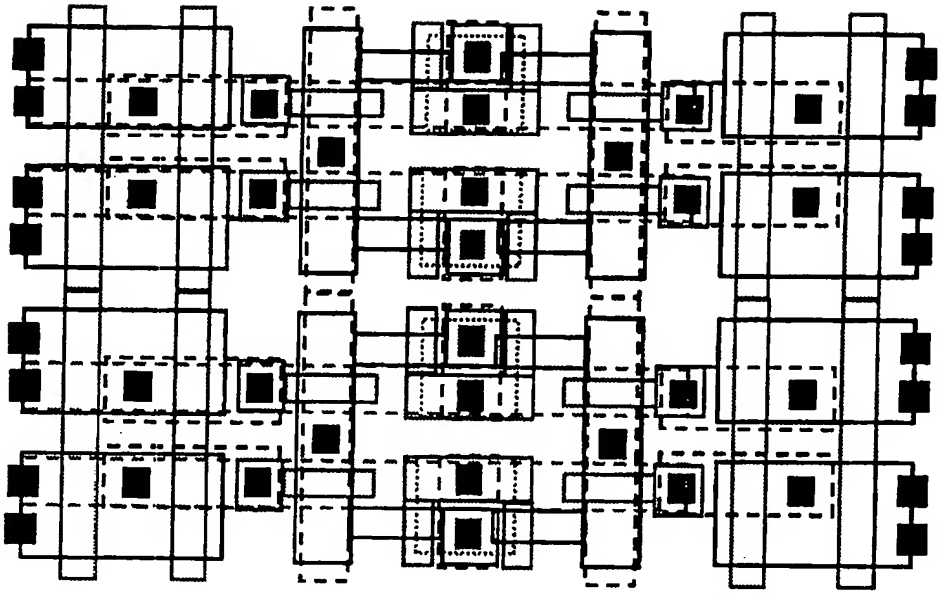

Fig 11